BRIEF FOR APPELLEE DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT

2006-1230
(Serial No. 09/885,217)

IN RE MICRON TECHNOLOGY, INC.

Appeal from the United States Patent and Trademark Office,
Board of Patent Appeals and Interferences.

JOHN M. WHEALAN
Solicitor

SYDNEY O. JOHNSON, JR.
JOSEPH G. PICCOLO
Associate Solicitors

P.O. Box 15667
Arlington, Virginia 22215
571-272-9035

Attorneys for the Director of the United States Patent and Trademark Office

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Representative Claim 223

223. A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

(i) an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing a current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage; and

(ii) a unity gain amplifier responsive to said reference signal for producing the reference voltage.

A2 (underlining added to reflect the only limitations in dispute and numbers added).

TABLE OF CONTENTS

I. STATEMENT OF THE ISSUE 1

II. STATEMENT OF THE CASE 2

III. STATEMENT OF THE FACTS 2

A. Micron's Claimed Invention 2

B. Anticipated Prior Art: Morishita 3

C. The Examiner's Answer And The Board's Decision 6

IV. SUMMARY OF THE ARGUMENT 8

V. ARGUMENT 9

A. Standard of Review 9

B. Morishita Anticipates The Claimed Voltage Reference Circuit 10

1. Morishita Discloses A Reference Signal That Has A Desired Relationship With An External Voltage. 12

2. Morishita Discloses A Unity Gain Amplifier As Broadly Claimed 16

a. The Claimed Unity Gain Amplifier Merely Requires An Amplifier Whose Output Voltage Equals The Input Voltage (Vout/Vin = 1) 16

b. Morishita Expressly States That The Output Voltage Is "Maintained At" The Input Voltage (Vout/Vin = 1) 17

c. Micron's Arguments That The Amplifier In Morishita Is Not A Unity Gain Amplifier Are Unavailing 19

i. By Teaching Vout = Vin, Morishita Discloses A Unity Gain Amplifier 19

ii. Micron's Gain = 1 21

iii. The Nominal Differences Between The Output Voltage And The Input Voltage Do Not Signify A Lack Of Unity Gain 22

iv. Micron's "House Water Tank" Hypothetical Is Not Analogous To The Amplifier In Morishita 23

VI. CONCLUSION 25

TABLE OF AUTHORITIES

Cases

Amer. Acad. of Sci. Tech. Ctr., In re, 367 F.3d 1359 (Fed. Cir. 2004).....13

Berg, In re, 320 F.3d 1310 (Fed. Cir. 2003).....18

Bigio, In re, 381 F.3d 1320 (Fed. Cir. 2004) 13

Consolidated Edison Co. v. Nat'l Labor Relations Bd., 305 U.S. 197 (1938).....10

Cybor Corp. v. FAS Techs., Inc., 138 F.3d 1448 (Fed. Cir. 1998) (*en banc*).....9

Elmer v. ICC Fabricating, Inc., 67 F.3d 1571 (Fed. Cir. 1995).....10

Gartside, In re, 203 F.3d 1305 (Fed. Cir. 2000).....9, 10

Hiniker Co., In re, 150 F.3d 1362 (Fed. Cir. 1998).....14

Hyatt, In re, 211 F.3d 1367 (Fed. Cir. 2000).....9

Jolley, In re, 308 F.3d 1317 (Fed. Cir. 2002) 10

Laitram Corp. v. Cambridge Wire Cloth Co., 863 F.2d 855 (Fed. Cir. 1988).....14

Morris, In re, 127 F.3d 1048 (Fed. Cir. 1997). 9, 16

Oetiker, In re, 977 F.2d 1443 (Fed. Cir. 1992). 20

RF Del. v. Pac. Keystone Techs., Inc., 326 F.3d 1255 (Fed. Cir. 2003).....14

Schreiber, In re, 128 F.3d 1473 (Fed. Cir. 1997).....10

Thrift, In re, 298 F.3d 1357 (Fed. Cir. 2002).....13

Young, In re, 927 F.2d 588 (Fed. Cir. 1991).....3

Zletz, In re, 893 F.2d 319 (Fed. Cir. 1989).....16

STATEMENT OF RELATED CASES

The Director is not aware of any other appeal involving the underlying Board of Patent Appeals and Interferences decision in this case that was previously before this or any other appellate court. The Director is also not aware of any pending case in this or any other court that will directly affect, or be directly affected by, this Court's decision in this appeal.

BRIEF FOR APPELLEE DIRECTOR OF THE
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IN RE MICRON TECHNOLOGY, INC.

Appeal from the United States Patent and Trademark Office,
Board of Patent Appeals and Interferences.

I. STATEMENT OF THE ISSUE

Although Micron's application contained a specification with over 200 pages, and over 500 claims, this appeal involves one claim (claim 223), directed to a voltage reference circuit. The Board found that Morishita anticipated representative claim 223. On appeal, Micron only disputes Morishita teaches two of the claimed limitations (i) a reference signal having a desired relationship with an external voltage, and (ii) a unity gain amplifier. Thus, the two issues on appeal are whether substantial evidence supports the Board's determination that Morishita teaches these two limitations.

MICRON FIGs. 36A1, 36A2, 36A3

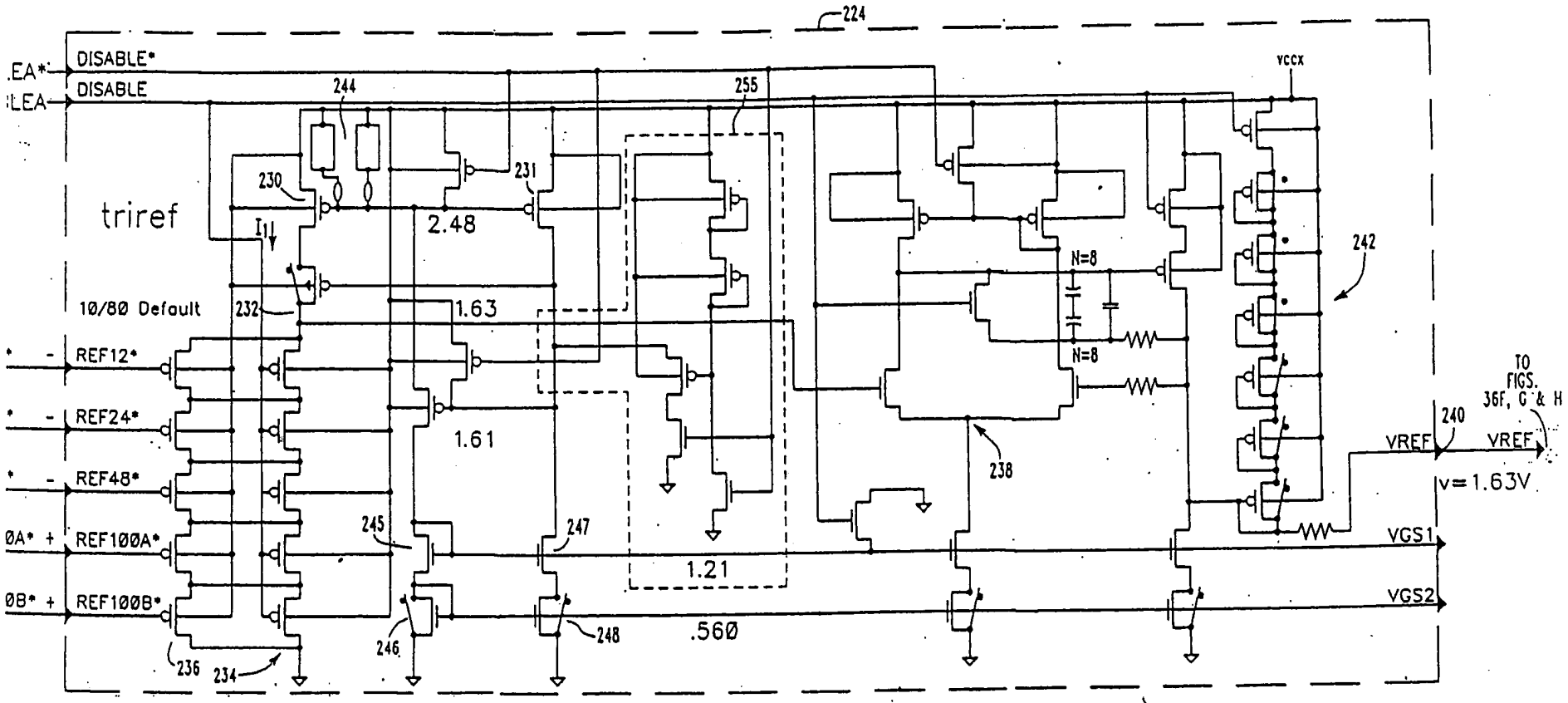


FIG. 36A1 FIG. 36A2 FIG. 36A3

II. STATEMENT OF THE CASE

This appeal involves Micron's patent application No. 09/885,217. The Examiner rejected claims 223, 225, 228-237, 247-250, 496, and 499-515 on multiple grounds as anticipated and obvious. The Board of Patent Appeals and Interferences (Board) affirmed the rejections. Micron now appeals the Board's decision to this Court.

III. STATEMENT OF THE FACTS

A. Micron's Claimed Invention

The claims on appeal relate to a voltage reference circuit that generates a reference voltage. The circuit is comprised of an active voltage reference circuit which produces a reference signal that is responsive to an external voltage. *See* A85, Figs. 36A1, 36A2, 36A3 on the opposite page; A682, lines 14-18. The active voltage reference circuit produces a desired relationship between the reference signal and the external voltage. A683, lines 4-5. The reference signal is then applied to a unity gain amplifier. A682, lines 25-26. The output of the unity gain amplifier is a reference voltage. *Id.* According to Micron's specification, using the unity gain amplifier improves overall voltage characteristics. A683, lines 8-10.

Representative claim 223 (the only claim Micron argues on appeal) broadly recites:

223. A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

(i) an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing a current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage; and

(ii) a unity gain amplifier responsive to said reference signal for producing the reference voltage. A2 (underlining added to reflect the only limitations in dispute and numbers added).[1]

B. Anticipated Prior Art: Morishita

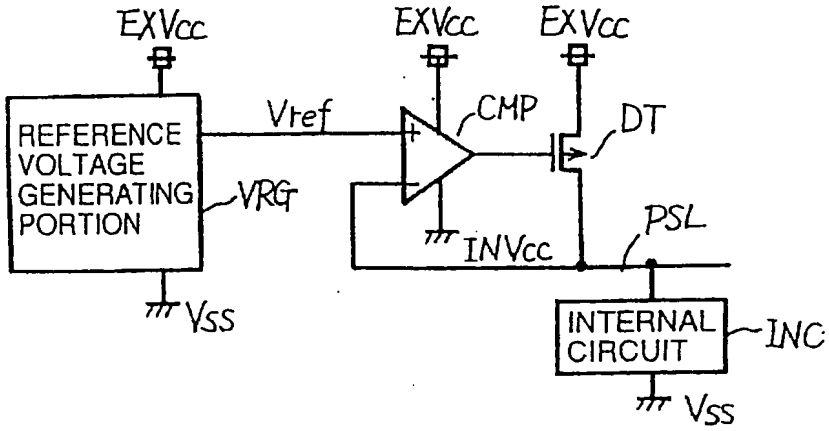
Micron utilizes terms in its claim that are similar to the ones Morishita uses to describe various aspects of the circuits he discusses. In an attempt to clarify and organize this discussion, we have provided the following chart illustrating key features.

Micron's claimed terms	Morishita
Reference Signal (voltage input into the amplifier)	Reference Voltage Vref (voltage input into the amplifier)
Reference Voltage Vref (voltage output from the amplifier)	Internal Voltage INVcc (voltage output from the amplifier)

[1] In his brief before the Board, Micron argued that all of the claims on appeal stand or fall with claim 223. A72. Similarly, in its brief to this Court, Micron only argued the merits of claim 223. Thus, all claims stand or fall with representative claim 223. *In re Young*, 927 F.2d 588, 590 (Fed. Cir. 1991).

MORISHITA PRIOR ART

FIG. 17 PRIOR ART



Morishita is directed to a constant current generating circuit. Before discussing his claimed invention, Morishita discusses a prior art circuit, which is commonly used in memory chips. A236, col. 1, lines 66-67. As shown in Figure 17 (opposite page), the circuit in Morishita has two stages. A234. The first stage includes voltage generator VRG, and the second stage includes comparator CMP, transistor DT, and internal circuit INC.

First Stage: The voltage generator VRG is comprised of a constant current generator CCG which generates a current based on current mirrors TP3 and TP4. *See* A235, Fig. 19; A237, col. 3, lines 34-38. The current flows through a diode stack CVC that has an adjustable impedance. A237, col. 4, lines 10-15; A238, col. 6, lines 10-11. The voltage generator VRG receives external voltage EXVcc, and generates a reference voltage Vref that is independent of the external voltage EXVcc when the external voltage EXVcc is at least at a prescribed voltage level. A236, col. 2, lines 2-5, 16-20.

Second Stage: The comparator CMP is comprised of a differential amplifier for amplifying the difference in the voltages applied at the (+) and (-) inputs. A237, col. 3, lines 22-25. The signal output from the comparator CMP controls transistor DT, which varies the amount of current flowing from external voltage EXVcc to line PSL. A236, col. 2, lines 10-15. The

current on the line PSL operates with the internal circuit INC to produce a voltage on the line PSL, namely, internal voltage INVcc. A236, col. 2, lines 34-36. The internal voltage INVcc is input into the (-) input of the comparator CMP though the feedback loop. A234, Fig. 17. The reference voltage Vref enters the (+) input of the comparator CMP. A234, Fig. 17.

Morishita explains that to ensure that the prior art circuit is reliable and has low power consumption, it is designed so that the internal voltage INVcc is maintained at the reference voltage Vref level. A236, col. 1, lines 44-47 and col. 2, lines 21-34. If the internal voltage INVcc is higher than the reference voltage Vref, then the comparator CMP output signal is high. A236, col. 2, lines 23-25. This signal causes the conductance in the transistor DT to decrease so that less current flows through transistor DT from the external voltage EXVcc to the line PSL. A236, col. 2, lines 28-32. The internal circuit INC in turn draws the decreased current on the line PSL. A236, col. 2, lines 34-36. As a result, the internal voltage INVcc is decreased until it matches the reference voltage Vref.

On the other hand, if the internal voltage INVcc is lower than the reference voltage Vref, then the comparator CMP output signal is low, and the conductance in the transistor DT is increased to allow more current to flow through the transistor DT from the external voltage EXVcc to the line

PSL. A236, col. 2, lines 21-23, 25-28; A237, col. 3, lines 14-21. By increasing the current, the internal voltage INVcc is increased until it equals the reference voltage Vref.

C. The Examiner's Answer And The Board's Decision

The Board affirmed the Examiner's rejection of representative claim 223 because it was anticipated by Morishita. The Examiner found that Morishita discloses a voltage reference circuit that is responsive to external voltage EXVcc and supplies an internal voltage INVcc. A56. The voltage reference circuit includes voltage generator VRG which receives the external voltage EXVcc and produces a reference voltage Vref having a desired relationship with the external voltage EXVcc. *Id.* The voltage generator VRG is comprised of a current source TP4 functioning with a current mirror TP3 and TP4 for providing current to a diode stack CVC that has an adjustable impedance. A57.

The Examiner found that Morishita also discloses, next to the voltage generator VRG, an amplifier comprised of comparator CMP and transistor DT. The Examiner noted that it is "well known" in the art that a unity gain amplifier is an amplifier with a gain equal to one. A63. The Examiner determined that for the amplifier in Morishita, the gain = Vout/Vin, *i.e.,* the internal voltage INVcc/reference voltage Vref. A64. The Examiner

recognized that Morishita states that the prior art circuit "maintains the internal voltage INVcc at the reference voltage Vref level." A64 (quoting Morishita, A236, col. 2, lines 32-34). Therefore, the Examiner found that the internal voltage INVcc is equal to reference voltage Vref, and that the gain of the amplifier is one or unity. A64.

The Examiner further found that Morishita discloses that the reference voltage Vref is "independent of the external voltage EXVcc when the external voltage EXVcc is at least at a prescribed voltage level." A57 (citing Morishita, A236, col.2, lines 17-20). Thus, the Examiner reasoned that "when the voltage EXVcc is lower than the prescribed voltage level, the reference voltage is dependent on the external supply voltage EXVcc." A57.

The Board agreed with the Examiner's findings. A5. Specifically, the Board similarly found that the circuit in Figure 17 of Morishita illustrates and meets Micron's voltage reference circuit of claim 223. A6. The Board also found that Morishita discloses an amplifier comprised of the comparator CMP and transistor DT. A7. The Board determined that the internal voltage INVcc is maintained at the level of reference voltage Vref. A7. Accordingly, the Board found that the amplifier in Morishita (*i.e.*, comparator CMP coupled with the transistor DT) is a unity gain amplifier. A7.

The Board rejected Micron's argument that Morishita does not disclose the "desired relationship" limitation because the reference signal is not produced until the external voltage EXVcc exceeds a prescribed level. A7. The Board found that even if Micron is correct about how Morishita's reference signal operates, "the fact alone that the reference signal is not produced until the external voltage EXVcc exceeds a prescribed level establishes . . . a desired relationship with such external voltage." A7-8. Under these operating conditions, the Board further found that reference voltage Vref is dependent upon the external voltage EXVcc since the reference voltage Vref is produced when the external voltage EXVcc attains a certain voltage level. A8.

IV. SUMMARY OF THE ARGUMENT

Substantial evidence supports the Board's conclusion that representative claim 223 is anticipated by Morishita. Micron claims a voltage reference circuit with an active reference circuit that produces a reference signal that has a desired relationship with an external voltage, and a unity gain amplifier (an amplifier with a gain of one). Morishita teaches that the reference voltage is independent of the external voltage when the external voltage exceeds a prescribed voltage. Thus, the relationship between the reference

voltage and the external voltage is dependence until a certain external voltage is reached, and then independence.

In addition, Morishita expressly states that its circuit has an output voltage that is "maintained at" its input voltage. Hence, Morishita discloses an amplifier that has a gain equal to one (*i.e.*, gain = Vout/Vin = 1). Therefore, Morishita anticipates representative claim 223.

V. Argument

A. Standard of Review

Micron has the burden of showing that the Board committed reversible error with respect to either a legal conclusion or a factual finding. *In re Gartside*, 203 F.3d 1305, 1315-16 (Fed. Cir. 2000). Claim construction is a question of law that this Court reviews *de novo*. *Cybor Corp. v. FAS Techs., Inc.,* 138 F.3d 1448, 1456 (Fed. Cir. 1998) (*en banc*). Under this standard, the Court reviews the Board's interpretation of disputed claim language to determine whether it is "reasonable." *In re Morris*, 127 F.3d 1048, 1055 (Fed. Cir. 1997).

Anticipation is a question of fact. *In re Hyatt*, 211 F.3d 1367, 1371-72 (Fed. Cir. 2000). The Board's factual determinations are upheld unless they are not supported by substantial evidence. *Id.* at 1372. This Court has defined substantial evidence as that which "a reasonable mind might accept

as adequate to support a conclusion." *Gartside*, 203 F.3d at 1312 (quoting *Consolidated Edison Co. v. Nat'l Labor Relations Bd.*, 305 U.S. 197, 229-230 (1938)). "[W]here two different inconsistent conclusions may reasonably be drawn from the evidence in the record, an agency's decision to favor one conclusion over the other is the epitome of a decision that must be sustained upon review for substantial evidence." *In re Jolley*, 308 F.3d 1317, 1329 (Fed. Cir. 2002).

B. Morishita Anticipates The Claimed Voltage Reference Circuit

The anticipation analysis is a two-step process. First, the claims must be properly construed. *Elmer v. ICC Fabricating, Inc.*, 67 F.3d 1571, 1577 (Fed. Cir. 1995). Second, all of the limitations of the claims must be disclosed in a single prior art reference. *In re Schreiber*, 128 F.3d 1473, 1477 (Fed. Cir. 1997).

Representative claim 223 includes (i) an active reference circuit that produces a reference signal that is dependent upon an external signal and has a desired relationship with an external voltage, and (ii) a unity gain amplifier. The active reference circuit has a current source and a current mirror that produces a current to a diode stack having an adjustable impedance. Morishita discloses an active reference circuit that receives an external voltage, produces a reference signal that is dependent upon the

external voltage, and includes a current source having a current mirror that provides a current to a diode stack having an adjustable impedance. The following chart illustrates that Morishita teaches every limitation of representative claim 223:

Representative Claim 223	**Morishita**
an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage, said active reference circuit comprising a current source utilizing a current mirror for providing current to a diode stack having an adjustable impedance, wherein said reference signal is dependent upon said external voltage	Fig. 19 shows: an active reference circuit (VRG) for receiving the external voltage (EXVcc) and for producing a reference signal (Vref) having a desired relationship with the external voltage (A236, col. 2, lines 16-20), said active reference circuit comprising a current source (TP4) utilizing a current mirror (TP3 and TP4) for providing current (I) to a diode stack (CVC) having an adjustable impedance, wherein said reference signal is dependent upon said external voltage. A5; A56-57; A235, Fig. 19; A236, col. 2, lines 16-20.
Unity Gain Amplifier	Unity Gain Amplifier has a gain = Vout/Vin = 1. A63. Morishita states that INVcc (Vout) is maintained at the Vref level (Vin). Col. 2, lines 31-34. Thus, INVcc/Vref = 1. A6-7.

Micron's only dispute is that Morishita does not teach the following two limitations: (i) a reference signal having a "desired relationship" with the external voltage; and (ii) a unity gain amplifier. Br. at 10, 14-18, and 21. However, as the Board properly found, Morishita expressly teaches both of these limitations.

1. Morishita Discloses A Reference Signal That Has A Desired Relationship With An External Voltage

Claim 223 broadly recites that the reference signal has a desired relationship with the external voltage. A2. Morishita's Figure 17 shows an external voltage EXVcc applied to voltage generator VRG to generate reference voltage Vref. *See* A234-235, Figs. 17 and 19. Morishita explains that when external voltage EXVcc is at least at a prescribed voltage, reference voltage Vref is independent of external voltage EXVcc. A236, lines 16-20. As a result, the Examiner and the Board found that when external voltage EXVcc is below the prescribed voltage, the reference voltage Vref is dependent on external voltage EXVcc. A5; A57. Thus, the desired relationship between the two voltages is clear – dependence until external voltage EXVcc reaches a certain voltage, after which, independence. Accordingly, the Board properly agreed with the Examiner that the reference voltage Vref taught in Morishita has a desired relationship with the external voltage EXVcc in the same way in which the claimed reference signal has a "desired relationship" with the external voltage.

Micron argues that Morishita does not disclose a reference signal having a desired relationship with the external voltage. Br. at 20. In Micron's view, the "desired relationship" is the shape of the reference signal illustrated in Figure 36B. *Id.* Micron's reasoning is misplaced for two

reasons. First, claim 223 is broadly written such that it encompasses any type of desired relationship between a reference signal and an external voltage. Indeed, the claim merely requires the reference signal to have a "desired relationship" with the external voltage. Nowhere does the claim limit the "desired relationship" to any particular type of "relationship," much less the one illustrated in Figure 36B.

Moreover, there is no evidence, and Micron points to none, showing that it disclaimed broader definitions of the claimed "desired relationship." "Absent claim language carrying a narrow meaning, the PTO should only limit the claim based on the specification or prosecution history when those sources expressly disclaim the broader definition." *In re Bigio*, 381 F.3d 1320, 1325-26 (Fed. Cir. 2004) (rejecting hairbrushes for the scalp where there was not express disavowal of other types of hairbrushes in the specification); *In re Amer. Acad. of Sci. Tech. Ctr.* 367 F.3d 1359, 1365 (Fed. Cir. 2004) (rejecting appellant's arguments that the claim term "user computer" should be limited to only "single-user computers" where no express disavowal of "multi-user computers"); *see also In re Thrift*, 298 F.3d 1357, 1364 (Fed. Cir. 2002) (rejecting appellant's arguments that the term "speech user agent" should be interpreted more narrowly where the term was

used in the claim without any modifiers and no express disavowal in the specification).

Second, it is axiomatic that the name of the game is the claim, *In re Hiniker Co.*, 150 F.3d 1362, 1369 (Fed. Cir. 1998), and that claims are not limited to a preferred embodiment described, *RF Del. v. Pac. Keystone Techs., Inc.*, 326 F.3d 1255, 1263 (Fed. Cir. 2003). In fact, "[r]eferences to a preferred embodiment, such as those often present in a specification, are not claim limitations." *Laitram Corp. v. Cambridge Wire Cloth Co.*, 863 F.2d 855, 865 (Fed. Cir. 1988). As Micron admits in its brief, Figure 36B "illustrates one example of how the reference signal may . . . have a desired relationship with the external voltage." Br. at 20 (emphasis added). Hence, it is a preferred embodiment of the "desired relationship." If Micron wanted to claim the "desired relationship" in Figure 36B, it should have amended its claims to recite the relationship depicted in this figure while its application was pending before the USPTO. Micron chose not to do so. As a result, this Court should decline to limit the claims to the relationship illustrated in Figure 36B.

Next, Micron asserts that Morishita is missing the "desired relationship" limitation because Morishita teaches that the reference voltage Vref is not operative until the external voltage reaches a predetermined

voltage, but thereafter, the circuit operates independently of the external voltage EXVcc. Br. at 21 (citing A236, col. 2, lines 16-20). Even assuming arguendo, as the Board did, that Morishita operates as Micron suggests, the "desired relationship" limitation would still be satisfied by Morishita. A7. Morishita teaches that once the external voltage EXVcc exceeds a prescribed voltage, the reference voltage Vref is a constant voltage that is independent of the external voltage EXVcc. A236, col. 2, lines 16-20; A238, col. 6, lines 12-15. Thus, if the reference voltage Vref is not active until the external voltage EXVcc is at least at a predetermined voltage, then the "desired relationship" is the reference voltage Vref being (1) zero when the external voltage EXVcc is less than a predetermined voltage, and (2) constant after the external voltage EXVcc exceeds the predetermined voltage.

Finally, Micron argues that it was legal error for the Board to construe the claimed "dependent upon" and "desired relationship" to mean the same thing. Br. at 22. However, Micron misapprehends the Board's decision. The Board found distinct meanings for each of these terms. A7-8. The Board found that when the external voltage EXVcc is lower than a predetermined voltage, the reference voltage Vref is dependent on the external voltage EXVcc. A5; A8; A57. Thus, the "dependent upon" limitation occurs when the external voltage EXVcc is between zero volts and

a predetermined voltage. Indeed, in its brief to this Court, Micron concedes that Morishita teaches that the reference voltage Vref is "dependent upon" the external voltage EXVcc as claimed in the "dependent upon" limitation of representative claim 223. Br. at 21.

The Board found a separate definition for the "desired relationship" language. The Board found that the "desired relationship" resides in the fact that the reference voltage Vref is not generated until the external voltage EXVcc exceeds a predetermined voltage. A8. In other words, the "desired relationship" is two-fold. It exists when the reference voltage is below the predetermined voltage, and when the reference voltage is at and above the predetermined voltage. Accordingly, the Board did not give the "dependent upon" and "desired relationship" the same meaning.

2. Morishita Discloses A Unity Gain Amplifier As Broadly Claimed

a. The Claimed Unity Gain Amplifier Merely Requires An Amplifier Whose Output Voltage Equals The Input Voltage (Vout/Vin = 1)

During *ex parte* prosecution, the USPTO is required to give claims their broadest reasonable interpretation consistent with the specification. *Morris*, 127 F.3d at 1055. It is presumed that the words in a patent claim have their ordinary and customary meaning unless the applicant has

provided a clear alternative definition. *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989).

Representative claim 223 broadly recites a "unity gain amplifier" that responds to a reference signal and produces a reference voltage. A2. As the Examiner found, it is "well known" that a unity gain amplifier is simply an amplifier with a gain equal to one. A63. Micron's specification does not give any alternative definition. Micron agrees with this definition. Br. at 6 ("A unity gain amplifier is an amplifier having a gain of 'unity' such that the output signal is the same as the magnitude of the input signal."). Therefore, the Board properly adopted the Examiner's finding that the term "unity gain amplifier" means an amplifier whose gain is equal to one. In other words, gain = Vout/Vin = 1.

b. Morishita Expressly States That The Output Voltage Is "Maintained At" The Input Voltage (Vout/Vin = 1)

As shown in Figure 17, Morishita discloses a comparator CMP comprised of a differential amplifier with (+) and (-) inputs. A237, col. 3, lines 22-23. The output of the comparator CMP is connected to the transistor DT that simply acts like a gate that allows current to pass to the line PSL. A237, col. 3, lines 22-31. The current on the line PSL flows through the internal circuit INC to produce internal voltage INVcc. A236, col. 2, lines 34-36. The internal voltage INVcc travels on the feedback loop

to the (-) input of the comparator CMP. *See* A234, Fig. 17. The voltage entering the (+) input is reference voltage Vref. *Id.* Given that transistor DT is on the path which forms the feedback loop that sends the internal voltage INVcc into an input of the comparator CMP, the transistor DT coupled with the comparator CMP forms an amplifier. A5; A64; A234, Fig. 17.

Additionally, the gain of the amplifier formed by comparator CMP and transistor DT is one. Amplifier gains are simply the ratio of the output voltage and the input voltage (*i.e.*, gain = Vout/Vin). A5; A64. Thus, here, the amplifier gain equals the ratio of the internal voltage INVcc and the reference voltage Vref (*i.e.*, gain = INVcc/Vref). Morishita expressly teaches that the internal voltage INVcc is maintained at the level of the reference voltage Vref. A236, col. 2, lines 31-34 (the circuit in Fig. 17 "maintains the internal power supply voltage INVcc at the reference voltage Vref level"). As a result of Morishita stating that the internal voltage INVcc is "maintained at" the reference voltage, the Board properly agreed with the Examiner that the internal voltage INVcc equals the reference voltage Vref. A5; A64. *See e.g., In re Berg*, 320 F.3d 1310, 1315 (Fed. Cir. 2003) ("As persons of scientific competence in the fields in which they work, examiners and administrative patent judges on the Board are responsible for making findings, informed by their scientific knowledge, as to the meaning of prior

art references to persons of ordinary skill in the art"). Therefore, the Board correctly found that the amplifier in Morishita is a unity gain amplifier. A7.

c. Micron's Arguments That The Amplifier In Morishita Is Not A Unity Gain Amplifier Are Unavailing

According to Micron, the amplifier in Morishita does not produce a unity gain because (i) Morishita does not use the words "unity gain amplifier" to describe the elements comprising the amplifier (comparator CMP coupled with transistor DT), (ii) the gain is greater than one or zero, (iii) the internal voltage INVcc is not always exactly equal to the reference voltage Vref, and (iv) the amplifier is similar to Micron's "house water tank" hypothetical which is not a unity gain amplifier. However, as fully explained below, none of these arguments is supported by the evidence.

i. By Teaching Vout = Vin, Morishita Discloses A Unity Gain Amplifier

Micron first suggests that the amplifier in Morishita is not a unity gain amplifier simply because Morishita does not refer to the combination of the comparator CMP and transistor DT as a "unity gain amplifier." Br. at 9, 17. Such an argument is, however, based solely on semantics. The amplifier, though comprised of comparator CMP and transistor DT, is substantially identical in structure to the embodiment taught in Micron's drawings for the

MORISHITA PRIOR ART

FIG.17 PRIOR ART

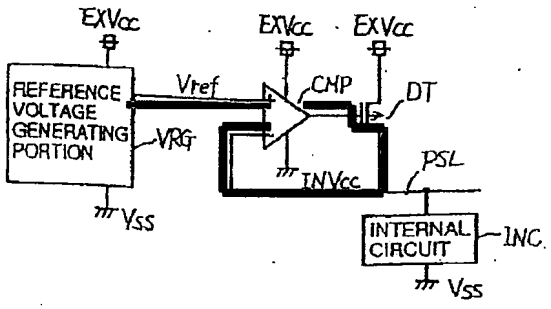
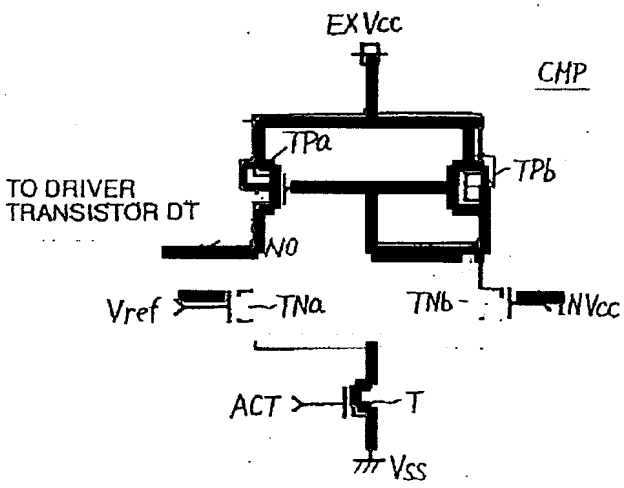
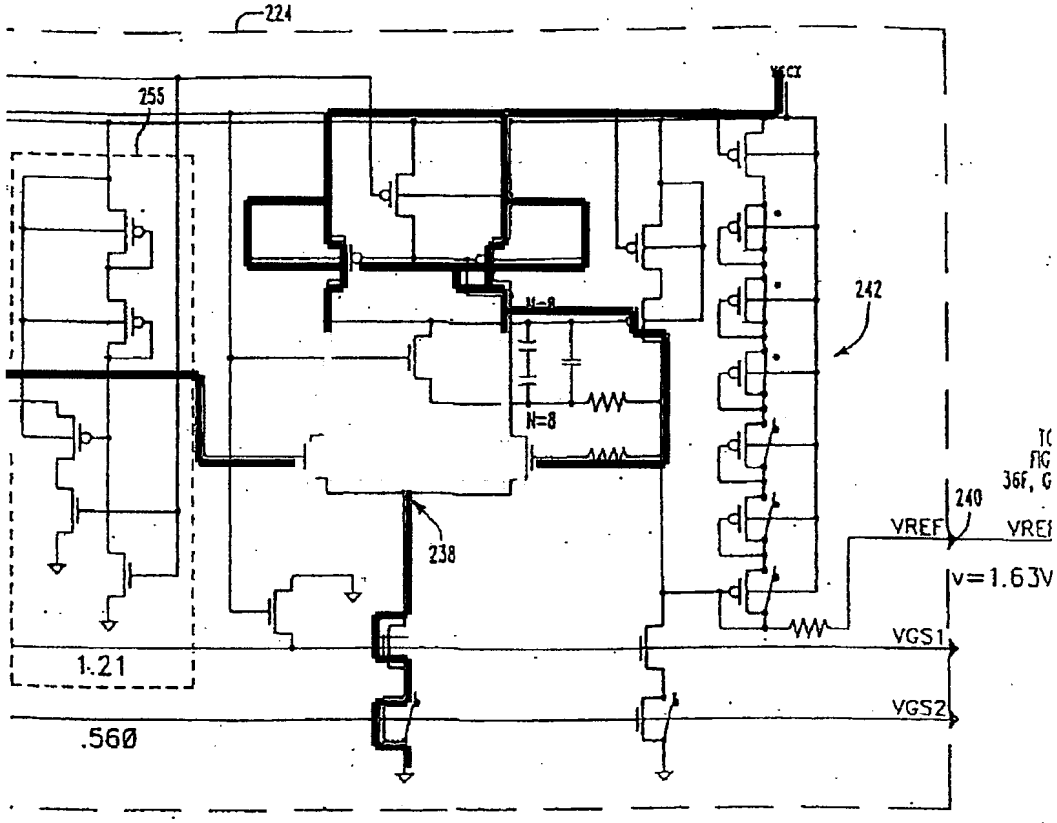


FIG.18 PRIOR ART



MICRON FIGs. 36A1, 36A2, 36A3



claimed unity gain amplifier. *Compare* A234, Fig. 17 and A235, Fig. 18 *with* A85, Fig. 36A2-3.

When the USPTO shows that a prior art invention is substantially identical to the claimed invention, the burden shifts to the applicant to show novelty. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). As shown on the opposite page, the claimed unity gain amplifier and the amplifier in Morishita both have (1) a differential amplifier comprised of transistors that determine the voltage difference at the inputs – yellow, (2) an external voltage source – pink, (3) a transistor to regulate the current from the external voltage source – dark green, (4) a feedback loop directing the output voltage into an input of the amplifier – orange, (5) a transistor to activate the amplifier – light green, and (6) a current mirror – light blue and dark blue. Given the striking similarities in the structures between the claimed unity gain amplifier and the amplifier in Morishita, it follows that the two perform the same function. Put another way, if the claimed amplifier functions as a unity gain amplifier, then so must the amplifier in Morishita. Micron's argument premised on semantics thus must fail since Micron did not present any evidence demonstrating an error in the Examiner's and Board's finding that the amplifier in Morishita is a unity gain amplifier.

ii. Morishita's Gain = 1

Micron argues that Morishita's amplifier does not teach a unity gain amplifier because the gain is either greater than one or zero. This argument is based on the assumption that if the output of the comparator CMP is very large, the transistor will be fully conductive. Br. at 15, 18. The problem is that Micron's assumption is inconsistent with Morishita's express teachings. Morishita does not disclose that when the comparator CMP is large, the transistor DT will be fully conductive. Rather, Morishita teaches that when the comparator output is large, the conductance in the transistor DT decreases to lower the amount of current flowing to the line PSL. A236, col. 2, lines 23-25, 28-30. As the internal circuit INC draws the reduced current from the line PSL, the internal voltage INVcc, which is the voltage across the line PSL, decreases. Since the comparator's output is large only when the internal voltage INVcc is higher than the reference voltage Vref, a small amount of current on the line PSL is needed to enable the internal voltage INVcc to decrease until it is at the reference voltage Vref. A236, col. 2, lines 23-25, 33-35.

Moreover, Micron is mistaken that if the signal produced by the comparator CMP is zero, the transistor DT is <u>non</u>-conductive. Br. at 13, 16, 18. If the comparator CMP is low, then the transistor DT is conductive

allowing a large supply of current onto line PSL. A236, col. 2, lines 22-23, 25-28. Consequently, when the internal circuit INC draws the large supply of current from the line PSL, internal voltage INVcc begins to increase until the internal voltage INVcc is at the reference voltage Vref. A236, col. 2, lines 33-35.

Furthermore, when the internal voltage INVcc is equal to the reference voltage Vref, the transistor DT is not non-conductive. Br. at 13, 16, 18. Instead, under this condition, the comparator CMP outputs a signal that instructs transistor DT to allow a sufficient amount of current to pass to the line PSL so that when the internal circuit INC draws from the current, the internal voltage INVcc will be maintained at the reference voltage Vref.

iii. The Nominal Differences Between The Output Voltage And The Input Voltage Do Not Signify A Lack Of Unity Gain

Micron contends that just because the reference voltage and the internal voltage INVcc are equal to one another at some point in time does not mean that all of the circuitry between those two signals is a unity gain amplifier. Br. at 14. Although the internal voltage INVcc does not exactly equal the reference voltage Vref at all times due in part to the fact that the internal circuit INC draws from the internal voltage INVcc, Micron fails to appreciate that any difference between the two voltages is nominal. At the

precise moment the internal voltage INVcc begins to change from the level of the reference voltage Vref, the amount of current flowing through the transistor DT is varied until the internal voltage INVcc is once again at the reference voltage Vref. For example, suppose that the reference voltage Vref = 12.0 volts. If the internal voltage INVcc drops to 11.9 volts, then more current is delivered through the transistor DT until the internal voltage INVcc increases to 12.0 volts. Similarly, if the internal voltage INVcc increases to 12.1 volts, then less current passes through the transistor DT until internal voltage INVcc decreases to 12.0 volts. Since the variation is small, a person of ordinary skill in the art would deem the internal voltage INVcc to be effectively equal to the reference voltage Vref. Therefore, the small changes do not alter the Board's conclusion that the amplifier is a unity gain amplifier.

iv. Micron's "House Water Tank" Hypothetical Is Not Analogous To The Amplifier In Morishita

Somewhat surprisingly, Micron begins it argument, and spends a significant portion of its brief, directed to a "house water tank" hypothetical. Br. at 10-15, 18. Not only does Micron's hypothetical distract from the key inquiry – does Morishita teach an amplifier with a gain of one – it includes a significant feature not found in Morishita. Micron asserts that the house water tank that holds varying amounts of water depending on which

appliance is turned on is analogous to the line PSL in Morishita. Br. at 13. Contrary to Micron's assertion, line PSL is not a variable storage device. It does not store voltage for later discharge, like a capacitor. Instead, it is simply a line through which current flows that leads to the internal circuit INC. *See e.g.*, A236, col. 2, lines 31, 37. Morishita, in fact, does not disclose any variable components, unlike Micron's "house water tank" hypothetical. For this reason, Micron's "house water tank" hypothetical, albeit somewhat appealing on first blush, is misleading and plainly not analogous to the circuit in Morishita.

At the bottom, the issue before this Court is not whether Micron's hypothetical house water tank anticipates claim 223. Rather, it is whether the amplifier in Morishita teaches a unity gain amplifier. Both the Examiner and the Board found that it does. Thus, the Court should not be distracted by Micron's apparent attempt to confuse the disclosure of Morishita by its inapposite hypothetical.

VI. CONCLUSION

Because substantial evidence supports the Board's factfinding that Morishita anticipates Micron's claim 223, the Board's decision should be affirmed.

Respectfully submitted,

July 19, 2006

JOHN M. WHEALAN
Solicitor
SYDNEY O. JOHNSON, JR.
JOSEPH G. PICCOLO
Associate Solicitors

P.O. Box 15667
Arlington, VA 22215
571-272-9035

Attorneys for the Director of the United States Patent and Trademark Office

CERTIFICATE OF SERVICE

I certify that on July 19, 2006, I caused two copies of the foregoing BRIEF FOR APPELLEE DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE to be sent first class mail to:

EDWARD L. PENCOSKE
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500 GRANT STREET
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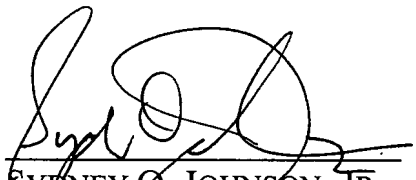

SYDNEY O. JOHNSON, JR.
Associate Solicitor